REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 1-24 are pending in the present application.

Claims 1-8, and 15-20 are objected to because of informalities.

Claims 2, 4, 9-15, and 21-24 are rejected under 35 U.S.C. §112, second paragraph.

Claims 16-21 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 3,604,911 ("Schmitt").

Claims 1, 3, and 5-8 are indicated as being allowable if rewritten to overcome their objections.

Claims 2, 4, and 9-15 are indicated as being allowable if rewritten or amended to overcome their 35 U.S.C. §112, second paragraph rejections.

Claims 22-24 are indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 4, 7, 9, 15, 16, and 21 have been amended. Support for amended claims 2, 4, 7, 9, 15, 16, and 21 is found on pages 4-31 of the specification, Figures 1-11, and claims 1-24 as originally filed. No new matter has been added.

Claims 1-8, and 15-20 are objected to because of informalities.

The Examiner states in part that

> Claim 1, line 9: "a first sequence" is suggested changing to "the first set"; and line 11: "a second sequence" is suggested changing to "the second set".
> Claim 7, line 1: "generating" is suggested changing to "to determine", "from a" is suggested changing to "from the"; line 2: "from a" is suggested changing to "from the", and "during a" is suggested changing to "during the".
> Claim 15, line 1: "determining" is suggested changing to "generating".
> Claim 16, lines 5 & 7, claim 20, line 2: "sets of sample values" is suggested changing to "sample sequences".

(10/29/2004 Office Action, p. 2)

With respect to claims 1 and 16, applicant respectfully submits that the terms "set of sample values" and "sequence of sample values" have distinct meaning and that the claim language should remain as presented. Page 20, line 14 to page 21, line 9 of the specification and Figure 6 describe an exemplary interpretation of the claim language according to an embodiment of the present invention.

Claims 7 and 15 have been amended.

Applicant respectfully submits that in view of the amendment to the claims and explanation of the claim language, the objection to the informalities has been overcome.

Claims 2, 4, 9-15, and 21-24 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2, 4, 9, and 21 have been amended.

Applicant respectfully submits that in view of the amendment to the claims, the claim rejections under 35 U.S.C. §112 have been overcome.

Claims 16-21 are rejected under 35 U.S.C. §102(b) as being unpatentable over Schmitt. In particular, the Examiner states that

> Regarding claims 16 & 18-19, in Fig. 1 Schmitt discloses sets of contiguous sample values in the received pattern shift register (element 30 of Fig. 2) of each M-bit segment comparator and sets of contiguous coefficients in the reference pattern shift register (element 32 of Fig. 2) of each M-bit segment comparator. In each/different recirculate time of Fig. 2 (d), each sample value in the received pattern shift register is exclusive OR (modulo 2 adder) with corresponding coefficient (Fig. 3).
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> . . .
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> Regarding claim 21, in Fig. 1 & Fig. 3, Schmitt discloses a correlator comprising M stage received pattern shift registers 30 (in elements 101 & 103) storing n sample values process in parallel, M stage reference pattern shift registers 32 (in elements 101 to 104) store up to 2n coefficients of code sequence; and elements 48, 50 and 52 in each segment comparator processing the sample values in each register 30 with corresponding

coefficients in registers 32 during different recirculate time as indicated in Fig. 3.

(10/29/2004 Office Action, p. 4).

Applicants respectfully submit that Schmitt does not render claim 16 or 21, as amended, unpatentable 35 U.S.C. §102(b).

Schmitt discloses a digital correlator for measuring the amount of agreement between two binary sequences comprising a plurality of cascade-connected segment comparators each operative to serially compare the bits within an M-bit segment of the sequences. A summing bus collects in parallel the comparison output signals of the segment comparators and applies them to a detector comprising an integrator and threshold circuit. Each segment comparator comprises a pair of M-bit shift registers each of which processes bits of a respective one of the binary sequences, a pair of exclusive OR gates for controlling serial loading and recirculation of respective registers, clock drive and feedback connections for recirculating the contents of both registers between the loading of each bit into one of the registers, and a modulo 2 adder for serially comparing the outputs of the registers (Schmitt Abstract).

It is submitted that Schmitt does not teach or suggest processing in parallel the sample values in each of the plurality of sample values that are accessed with corresponding coefficients that are accessed.

On the contrary, Schmitt discloses breaking correlation data and coefficients into separate sets and processing each set of correlation data and coefficients serially. Objects are attained by a digital correlator comprising a plurality of cascade-connected segment comparators each of which is operative to serially compare the bits within a selected segment of the two binary sequences to be correlated as one sequence is shifted in time with respect to the other (see col. 1, line 71 to col. 2, line 1).

In contrast, amended claim 16 states

> A method for managing a code sequence, comprising:
> accessing sets of n contiguous sample values that include sample values in a plurality of sample sequences;
> accessing sets of n contiguous coefficients; and
> processing in parallel the sample values in each of the plurality of sets of sample values that are accessed with corresponding coefficients that are accessed, where each of the plurality of sets of sample values are processed during a different time step.

(Amended Claim 16) (Emphasis added).

Claim 21 includes similar limitations. Claim 21 states

> A correlator unit, comprising:
> a plurality of n sample sequence registers that store sample values from a plurality of sample sequences that are processed in parallel, the plurality of n sample sequence registers storing sample values from one set of sample values of a plurality of sets of sample values from the plurality of sample sequences at a time;
> a plurality of 2n code sequence registers that store up to 2n coefficients from a code sequence; and
> a processing unit that processes the sample values in each of the plurality of sets of sample values in the plurality of n sample sequence registers in parallel with corresponding coefficients in the plurality of 2n code sequence registers, where each of the plurality of sets of sample values is processed during a different time step.

(Amended Claim 21) (Emphasis added).

Given that claims 17-20, depend from claim 16, it is likewise submitted that claims 17-20, are also patentable under 35 U.S.C. §102(b) over Schmitt.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections have been overcome. Accordingly, it is respectfully submitted that claims 1-24, as amended, should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: January 28, 2005

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